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ANALYSIS OF THE POTENTIATION DIGITAL-TO-ANALOG CONVERTER WITHOUT ACCOUNTING OF IMPERFECTION ITS BLOCKS

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***Abstract*—*Potentiation digital-to-analog converter with iterative additive correction of errors is described. Analysis of errors of this converter without accounting of imperfection its blocks was produced. Basic expressions for the calculation of these errors are listed. Author developed the potentiation digital-to-analog converter with iterative additive correction of errors. Test results and operation experience confirmed the correctness of the results of theoretical research.*

Index Terms—Integrator; potentiation digital-to-analog converter; iteratively additive correction of errors; imperfection of blocks; dynamics of the iterative process.

I. INTRODUCTION

In the information systems related to the collection, processing and transmission of information are essential measuring converters. The achievement of linearity of their functions transformation is very important for measuring converters application in such systems, and consequently for independence of static transformative characteristics from value of transformed quantity. Reduction of level of error measuring converters often plays a decisive role in solving the problem of creation of information systems such as automated information-measuring systems, automated control systems, pattern recognition, diagnosis or identification. It is provided by using special materials, application of special technology of its production or special design of converter elements performance (usage of more qualitative elements, application of screens, thermostats, etc.) [1], but this not always allows achieving the needed linearity of transfer function with sufficient accuracy.

In some cases by means of the measuring converters the transformation of one electric value into another is performed. Such values, for example, can be a DC voltage, current, capacitance, resistance and code.

Measuring converters, the input value that is the code and the output – voltage, known as Digital-to-Analog converter (DAC), has a wide application in information-measuring systems. DAC is one of the main blocks of almost any automated measuring system. The metrological parameters of the DAC is often largely determined by the metrological parameters of the entire measuring system.

II. PROBLEM STATEMENT

Based on its review of the principle of action potentiation transmitter block diagram is proposed by the author we obtain the equation conversions and basic expressions for determination of static and dynamic errors of the device, as well as an expression to determine the number of cycles of the converter required to achieve a given conversion error.

III. INCREASING THE ACCURACY OF MEASURING CONVERTERS

Let us consider a problem of increasing the accuracy of measuring converters.

Among the many methods to increase the accuracy of transducers important are structural methods [1].

Structural methods of improving the accuracy include use of functional circuits in which it is possible to eliminate or reduce the influence of some of the errors most unstable blocks and elements for the total error of the device. The total error is invariant to one or another error of individual blocks or their combination.

A significant place among structural methods to increase the accuracy of measuring converters occupy iterative methods of error correction based on a well-developed theory in mathematics iterative methods.

At the same time, the measurement technique is very widely used various integrating converters, due to their advantages such as high accuracy, noise immunity and sensitivity, simplicity, reliability, low cost, etc.

Combining methods of integrating conversion and additive iterative error correction has generated a method called by the author [2], [3] iteratively integrating conversion method (IICM) and devices using this method – iteratively integrating converters (IIC). Iteratively integrating converters usually combine the advantages of both of the above methods. Many of iteratively integrating converters, [4] possess high metrological parameters.

IV. OPERATION PRINCIPLE OF ITERATIVELY INTEGRATING CONVERTERS

Functioning of iteratively integrating converter is carried out cyclically. In each cycle two integration

values over given time intervals. Then follows by memorizing the results of integration by sample-and-hold device. The output quantity of sample-and-hold device fed to the output of measuring converter during the subsequent cycle of operation.

Thus, of the four values we have two values, which are integrated, and the other two values, which define the integration time. One of these values is the output value of the measuring converter.

The other three values, in general, are input. The increment of the output value of the integrator by integrating these two values have different signs. The process of establishing the value of the output of the transmitter is described by geometric progression.

This process is convergent under certain conditions. As a result, the transmitter is carried out additive iterative error correction conversion (more work iteratively integrating measuring converters discussed below).

In steady state operation output value through a corrective amendment, which accumulates on the integrator, is such that the product of each of integrable values and corresponding integration times are equalized with each other.

V. GENERALIZED BLOCK DIAGRAM OF ITERATIVELY INTEGRATING CONVERTER

Large number of IIC can be represented by the simplified generalized structural scheme shown in Fig. 1, which was offered by the author in work [2]. Here X is the input value; Y is the output value; OC is output converter, BC is back converter; K_{BC} is transfer coefficient of BC; SW1 and SW2 are switches, SH is sample-and-hold device; $T1$ is time interval of integration of the input variable X; $T2$ is time interval of integration of the output value $K_{BC}Y$. The values of $T1$ and $T2$, along with X are input values.

Consider the work of the generalized scheme for the simplest case, when X and Y are the time intervals. The work comes in cycles. Each cycle is a step of iteration. It consist of the integration time $T1$ by integrator I of variable X through a non-inverting input, integration time $T2$ by integrator I of variable Y through an inverting input and memorizing by the sample-and-hold device SH of the integrator output voltage upon receipt at the end of the cycle of strobe $T3$. This value enters through the output converter OC to output of transducer during the subsequent conversion cycle.

Without dwelling on the details of the dynamics of the iterative process of establishing an output value that will be discussed in detail below, we indicate only that after a few cycles of the transition process ends and the inverter output value is given by

$$Y = \frac{T1X}{T2K_{BC}}.$$

From this expression, which is an equation of the conversion of the IIC, it follows that the steady-state output value does not depend on the transformation coefficients of direct circuit blocks I, SH and OC (K_I, K_{SH} and K_{OC} respectively).

Another variant of the simplified generalized structural scheme is shown in work [5]. More complex generalized scheme of IIC is considered in detail in work [4].

VI. MEASURING CONVERTER CODE-VOLTAGE

The structural scheme of iteratively integrating code-voltage converter is shown in Fig. 2. Here RFG is reference frequency generator. CTIC is converter of code into the time interval; STI is shaper of time intervals; E_0 is reference voltage; $N1$ is the input code, U_{out} is the output voltage.

This DAC is an iteratively integrating code-voltage converter with intermediate transformation into the time interval. It consists of two parts. The first one is a purely digital (RFG, CTIC, STI). It shapes control pulses (time intervals): $T1$ is a variable which is proportional to the input code $N1$; $T2$ and $T3$ are the time intervals of constant duration. Second part of the code-voltage converter is an analog (I, SH, SW1 and SW2). This one is the actual iteratively integrating converter. It converts of the time interval to voltage. Its job is to being alternately cyclic closure of the switches SW1 and SW2 and in memorizing the output voltage of the integrator when the impulse $T3$ arrives. The operation of this device is described in detail in the work [2].

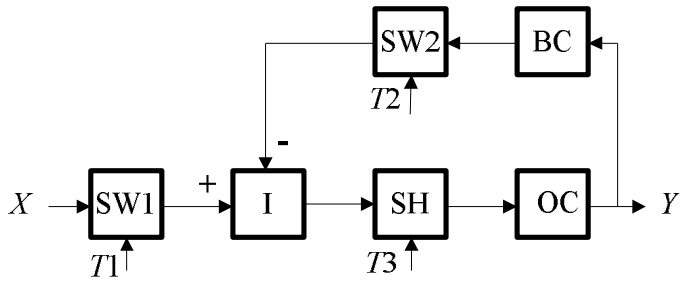

Fig. 1. Simplified generalized scheme of iteratively integrating converter

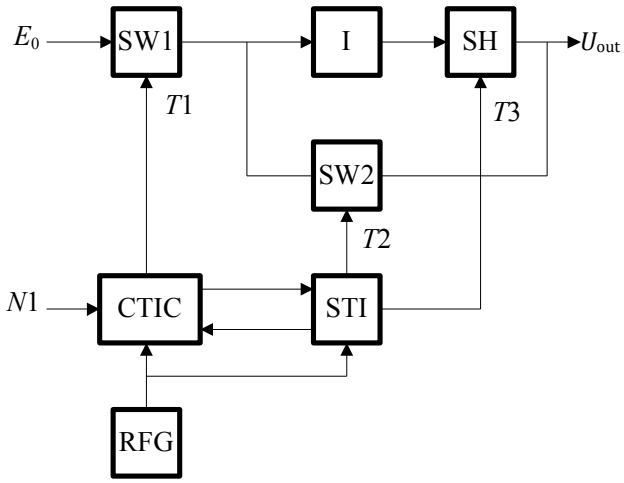

Fig. 2. Structural scheme of iteratively integrating code-voltage converter

Transition process of setting the output voltage in this converter after changing the input code is iterative, i.e., in each subsequent cycle of operation during the transient output voltage all the more approaches the value of the steady state and is described by

$$U_n = \frac{E_0 T1 K_{\text{RP}}}{RC} \sum_{j=1}^{n} Q^{j-1} + U_0 Q^n, \qquad (1)$$

where U_n is output voltage of the code-voltage converter after the end of nth cycle; K_{RP} is transfer coefficient of the sample-and-hold device SH; R and C are resistance and capacitance of the respective elements of the integrator I; j is cycle index after the change of code; $j = \overline{1,n}$; U_0 is output voltage of code-voltage converter before the first cycle; $Q = 1 - T2\, K_{\text{RP}}/RC$.

Expression (1) is the sum of geometric progression, convergent in case $|Q| < 1$, and decreasing at the same condition term $U_0 Q^n$. As a result, in the steady state output voltage of the iteratively integrating code-voltage converter is determined by the expression

$$U_\infty = \lim_{n\to\infty} U_n = \frac{E_0 T1}{T2} = \frac{E_0 N1}{N2}, \qquad (2)$$

where $N2$ is code, used to form time interval $T2$.

Expression (2) is the transformation equation of this DAC.

Condition for a maximum speed of convergence of the series (1), that is, the minimum duration of the transition process of setting the output voltage of the DAC is the equality $Q = 0$.

From (2) it follows that the transform coefficient of this DAC is independent of the transmission factors of the integrator I and sample-and-hold device SH. Whereby the stability requirements for them are low. The transform coefficient of this DAC depends only on the ratio of time intervals, that can be formed with very high accuracy. Thus, in this DAC time intervals ratio used instead of the resistance ratio [6], as it is done in a variety of DAC, representing all kinds of resistive circuit commutated by analog or electromechanical switches. As a result, practically precision resistors are abcent, and a number of presize analog switches is minimized (SW1 and SW2).

According to the firm Yokogawa Electric Works Ltd. [6] it created DAC which used as a multivalued DC voltage measure, capable of providing a resolution of about 0.00001 % (which corresponds to the 23 binary digits) and non-linearity of better than ± 0,00001 % (20 binary digits); the maximum output voltage equal to 1200 V.

The advantages of such DAC, compared with the DAC utilizing resistor circuit, should be attributed primarily elimination of errors due to aging of the resistance of resistors and a changes of resistance of switches [6], processability, resistance to impacts of temperature, simplicity and low cost (if necessary achieving comparatively higher accuracy) [7], low output resistance, ease of remote operation, possibility of constructing a MOS LSI, etc.

Another important advantage of this DAC is the ability to easily increase the number of discrete values of the output value. If in the resistive DAC this requires increasing the number of keys and precision resistors, in this DAC the increase of the number of possible output values is accompanied only by a rise of quantity of elements in the digital part. The presence of three inputs in this DAC (i.e. we have essentially computing device) allows you to build the various functional converters on its basis. One such device is a potentiation code-voltage converter (potentiation DAC). Further analysis of functional con-

verter based on iteratively integrating code-voltage converter is made on the example of the potentiation DAC.

VII. POTENTIATION DAC

Typically, the output analog value, for example, a DC voltage is directly proportional to the input code of the DAC [8]. However, there are cases where the DAC code performs non-linear transformation to an analog value. Type of nonlinearity depends on the task. For example, the DAC can generate a nonlinearity which is inverse to non-linearity of the sensor, thereby fulfilling the task of the linearization of the measuring path. It may be case when using the DAC implementing nonlinearity corresponding to a standard function. One such case is the construction of the DAC, in which the output voltage is directly proportional to the input code given in decibels.

Below we consider potentiation DAC which was offered by the author [4], [9] having a number of advantages in terms of its use in the automated measurement system. The structural scheme of iteratively integrating code-voltage converter with additive correction of errors is shown in Fig. 3. Here I is integrator; SH is sample-and-hold device; SW1 and SW2 are keys; RFG is reference frequency generator; CC1 and CC2 are code converters; CTIC1 and CTIC2 are converters of code into the time intervals; STI is shaper of time intervals; E_0 is reference voltage; $N = \lambda + \mu$ are the input code; U_{out} is output voltage; OC is output converter, BC is back converter.

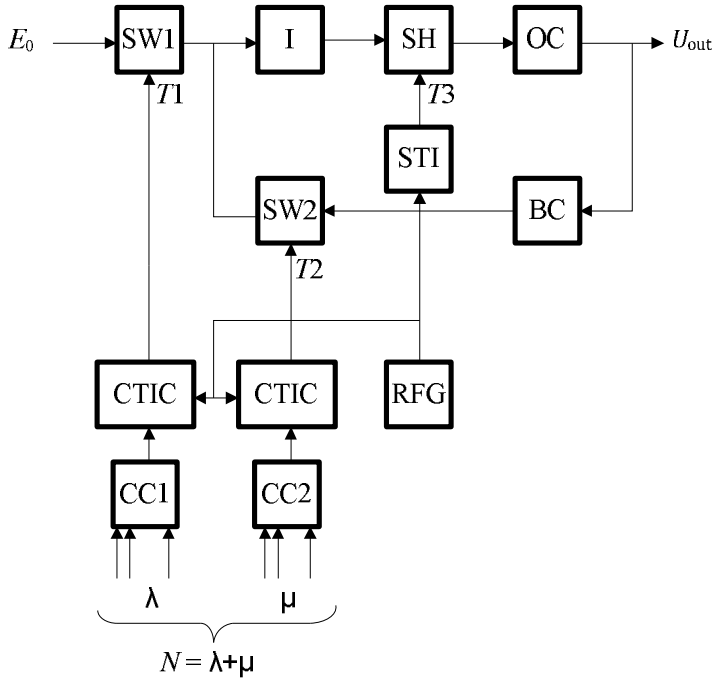

Fig. 3. Potentiation digital-to-analog converter

Nonlinearity which is realized in the converter corresponds to the operation of potentiation, i.e. function which is inverse to obtaining logarithm. The input code is given in decibels (dB). It determines the output voltage value relative to a value of U_0, corresponding to input code N = 0 dB, i.e. N (dB) = 20 lg U_{out} /U_0. From this expression we can obtain the equation of converting of this potentiation converter:

$$U_{out} = U_0 10^{N/20}.$$

If the submit an input code N as the sum of two terms (for example, integers and tenths) $N = \lambda + \mu$, conversion equation can be transformed to:

$$U_{out} = U_0 10^{\lambda/20} / 10^{-\mu/20}.$$

Functioning of iteratively integrating converter is carried out cyclically. In each cycle two integration values over given time intervals. Then follows the memorization of the result of integration by the sample and hold device

The output quantity of sample-and-hold device fed to the output of measuring converter during the subsequent cycle of operation.

This DAC is a code-voltage converter with intermediate transformation into the time interval. It consists of two parts. The first one is a purely digital (RFG, CTIC, STI). It shapes control pulses (time intervals): $T1$ is a variable which is proportional to the input code $N1$; $T2$ and $T3$ are the time intervals of constant duration. Second part of the code-voltage converter is an analog (I, SH, SW1 and SW2). This

one is the actual iteratively integrating converter. It converts of the time interval to voltage. Its job is to being alternately cyclic closure of the keys 1 and 2 and in memorizing the output voltage of the integrator when the impulse $T3$ arrives. The operation of this device is described in detail by the author [2], [4].

So after the ending of the first and second conversion cycles the output voltage U_{out} is equal to:

$$U_1 = (E_0 \lambda K_\lambda K_{SH} K_{RP} K_A / f_0 RC) - U_0 Q_H$$

and

$$U_2 = (E_0 \lambda K_\lambda K_{SH} K_{RP} K_A / f_0 RC)(1 - Q_H) - U_0 Q_H,$$

respectively, where: K_λ and K_μ, K_{SH}, K_{RP} and K_A – are transfer coefficients of the devices RFG, SH, OC and BC respectively, f_0 is reference frequency; R and C resistance and capacitance of integrators resistor and capacitor respectively; and

$$Q_H = 1 - \mu K_\mu K_{SH} K_{RP} K_A K_{VD} / f_0 RC.$$

Transition process of setting the output voltage in this converter after changing the input code is iterative, i.e. in each subsequent cycle of operation during the transient output voltage all the more approaches the value of the steady state and is described by

$$U_n = (E_0 \lambda K_\lambda K_{SH} K_{RP} K_A / f_0 RC) \sum_{j=1}^{n} Q_H^{j-1} - U_0 Q_H^n$$

$$= \frac{E_0 \lambda K_\lambda}{\mu K_\mu K_{VD}} (1 - Q_H) - U_0 Q_H^n = U_\infty - \Delta U Q_H^n.$$

where U_n is output voltage of the code-voltage converter after the end of nth cycle; $j = \overline{1,n}$.

Last expression consists of two parts. First of them is geometric progression, which converges at the condition $|Q_H| < 0$. Another one is the part $U_0 Q_H^n$ which is decreasing under the same condition.

If the condition $|Q_H| < 0$ is fulfilled, output voltage of the potentiation digital-to-analog converter at the steady-state condition ($n \to \infty$) is determined by the expression

$$U_\infty = \frac{E_0 \lambda K_\lambda}{\mu K_\mu K_{VD}} = \frac{E_0}{K_{VD}} 10^{(\lambda + \mu)/20},$$

where

$$K_\lambda = \frac{10^{\lambda/20}}{\lambda}, \qquad K_\mu = \frac{10^{-\mu/20}}{\mu}.$$

The relative error of conversion γ_n can be determined from the following expression

$$\gamma_n = \frac{U_n - U_\infty}{U_\infty} = \frac{\Delta U Q_H^n}{U_\infty},$$

where $\Delta U = U_\infty - U_0$.

From last expression can be determined the number of cycles n, corresponding to this error γ_n

$$n = \left[\frac{\ln \left| \frac{\gamma_n U_\infty}{\Delta U} \right|}{\ln |Q_H|} \right] + 1.$$

It should be emphasized that as it follows from the expressions, the quantity of numbers stored in the ROMs of code converters (CC1 and CC2) is determined not by the number of possible values of code N, as it was when potentiation digital-to-analog converter is builded by simple serial connection of nonlinear converter of codes and linear digital-to-analog converter (here, the number of possible values of N is equal to the product of λ and μ), but by the total number of possible values of λ and μ.

For instance, if N = 0; 0.1; ... 9.9, then the quantity of numbers in the ROM, for both cases equal to 100 and 20, respectively, and if N = 0.01; 0.02 ... 99.99, – 10 000 and 200. As you can see, the volume of ROM is sharply reduced, especially when a large number of gradations of N take place.

VIII. Conclusion

Potentiation digital-to-analog converter, i.e. DAC, in which the output voltage is directly proportional to the input code given in decibels, based on iteratively integrating code-voltage converter with iterative additive correction of errors, is considered. The obtained expressions allow you to create such digital-analog converter. The potentiation digital-to-analog converter with iterative additive correction of errors was developed by author. Test results and operation experience confirmed the correctness of the results of theoretical research. It must be emphasized that the device does not require the inclusion of devices such as a microprocessor, microcontroller or programmable logic controller and the quantity of numbers stored in the ROMs of code converters is very limited.

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І. Ю. Сергеєв. Аналіз потенціюючого цифро-аналогового перетворювача без урахування недосконалості його блоків

Розглянуто потенціюючий цифро-аналоговий перетворювач з ітераційною адитивною корекцією похибок. Виконано аналіз похибок цього перетворювача без урахування недосконалості його блоків. Наведено основні вирази для розрахунку його похибок. Результати випробувань і досвід експлуатації розробленого автором потенціюючого цифро-аналогового перетворювача з ітераційною адитивною корекцією похибок підтвердили правильність результатів теоретичних досліджень.

Ключові слова: інтегратор; потенціюючий цифро-аналоговий перетворювач; ітераційна адитивна корекція похибок; недосконаліть блоків; динаміка ітераційного процесу.

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И. Ю. Сергеев. Анализ потенцирующего цифро-аналогового преобразователя без учета несовершенства его блоков

Рассмотрен потенцирующий цифро-аналоговый преобразователь с итерационной аддитивной коррекцией погрешности. Выполнен анализ погрешностей этого преобразователя без учета неидеальности его блоков. Приведены основные выражения для расчета его погрешностей. Результаты испытаний и опыт эксплуатации разработаного автором потенцирующего цифро-аналогового преобразователя с итерационной аддитивной коррекцией погрешности подтвердили правильность результатов теоретических исследований.

Ключевые слова: интегратор; потенцирующий цифро-аналоговый преобразователь; итерационная аддитивная коррекция погрешностей; несовершенство блоков; динамика итерационного процесса.

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Направление научной деятельности: автоматизация технологических процессов, измерительные преобразователи.
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